Magnetron sputtered gadolinia-doped ceria diffusion barriers for metal-supported solid oxide fuel cells

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HIGHLIGHTS

- Sputtered gadolinia-doped ceria barriers implemented in metal-based SOFCs.
- Sr diffusion along column boundaries in the barrier layer is observed.
- Tuning deposition parameters makes 0.6 μm GDC effectively stop Sr diffusion.
- Area specific resistance of 0.34 Ω cm^2 is achieved for cells operating at 650 °C.

ARTICLE INFO

ABSTRACT

Gadolinia-doped ceria (GDC) thin films are deposited by reactive magnetron sputtering in an industrial-scale setup and implemented as barrier layers between the cathode and electrolyte in metal-based solid oxide fuel cells consisting of a metal support, an electrolyte of ZrO_2 co-doped with Sc_2O_3 and Y_2O_3 (ScYSZ) and a Sr-doped lanthanum cobalt oxide cathode. In order to optimize the deposition of GDC to obtain high electrochemical performance of the cells, the influence of film thickness and adatom mobility is studied. The adatom mobility is varied by tuning the deposition temperature and substrate bias voltage.

A GDC layer thickness of 0.6 μm is found to effectively block Sr diffusion when bias voltage and deposition temperature is tuned to promote dense coatings. The adatom mobility has a large influence on the film density. Low temperature and bias voltage result in underdense column boundaries which function as channels for Sr to diffuse to the GDC–ScYSZ interface. By tuning deposition temperature, bias voltage and film thickness area specific resistances down to 0.34 Ω cm^2 are achieved at cell tests performed at an operating temperature of 650 °C.

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1. Introduction

At intermediate temperatures, metal-supported solid oxide fuel cells (SOFCs) designs are of interest as an alternative to ceramic supported cells in view of their low materials cost and high robustness, which is advantageous both in the production line and in applications such as auxiliary power units [1]. During fabrication

of metal-supported cells, care must be taken to avoid corrosion of the steel components. This involves processing at lower temperatures or in reducing atmospheres. Therefore traditional cathodes developed for ceramic cells, such as (La,Sr)MnO$_{3-\delta}$ (LSM) and (La,Sr)(Co,Fe)O$_{3-\delta}$ (LSCF), cannot be transferred directly to metal-supported cells, as these cathodes requires sintering in air at 1000–1200 °C to achieve good adhesion of the cathode [1].

(La,Sr)CoO$_{3-\delta}$ (LSC) is another cathode material which has been found to be suitable for metal-supported cells as it sinters readily at temperatures below 900 °C and has a good electrochemical performance at intermediate temperatures [2,3]. However, LSC is incompatible with yttria-stabilized zirconia (YSZ) traditionally used for SOFC electrolytes, as strontium from the cathode reacts with zirconium from the electrolyte to form SrZrO$_3$ which has a low ionic

conductivity [4–6] and therefore a detrimental effect on cell performance. This reaction is known to take place during sintering at temperatures above 1000 °C [7] but has also been observed at intermediate temperatures down to 650 °C [5,8]. To avoid this reaction a gadolinia-doped ceria (GDC) barrier can be applied between electrolyte and cathode. Several studies have shown the suitability of GDC as a barrier for Sr diffusion [3,9–11]. GDC can be applied by screen printing, spraying, or tape casting followed by sintering at temperatures above 1200 °C. In itself GDC is an excellent ionic conductor but at these temperatures a solid solution of YSZ and GDC is formed which has significantly lower oxide ion conductivity than the pure form of both compounds [7,12,13]. Alternatively the GDC barrier can be applied by physical vapor deposition (PVD) techniques such as pulsed laser ablation [7], electron beam evaporation [14], or magnetron sputtering [3,11,15,16]. GDC barriers prepared by PVD techniques stops Sr diffusion better than barriers prepared by wet ceramic techniques. This may be due to higher density of such layers [3,11], which can be achieved at lower temperatures. Low-temperature deposition is particularly important for metal-supported cells, which cannot withstand as high temperatures as ceramic cells. When depositing on metal-supported cells it is reasonable to set 400 °C as the upper limit deposition temperature as the oxygen present for the reactive deposition process may oxidize the metal-support at elevated temperatures which reduces cell performance. When synthesizing GDC coatings for ceramic SOFCs high deposition temperatures are often used to grow coatings sufficiently dense to prevent Sr diffusion [11,17]. In a recent study, we showed using a model system that the main route for Sr diffusion in sputtered GDC films are along underdense column boundaries which can be densified and/or limited by increasing the adatom mobility [18]. Besides the deposition temperature, other ways to increase adatom mobility includes increasing the ionization degree of the plasma and applying a substrate bias. Especially the combination of elevated temperatures and the application of substrate bias have been found to be an effective method to tune the microstructure when depositing GDC for ceramic-supported SOFC [16].

In this work, the influence of substrate bias voltage, film thickness, and deposition temperature on reactively sputtered GDC barriers for metal-supported cells are investigated. The purpose of the study is twofold. First, we demonstrate how deposition of GDC can be tuned to form effective diffusion barriers to metal-supported cells. Furthermore, we prove the Sr diffusion mechanism to be as previously demonstrated in a model system [18].

2. Experimental details

GDC ($Ce_{0.9}Gd_{0.1}O_{2−\delta}$) coatings were deposited by reactive pulsed magnetron sputtering using a CC800/9 SinOx industrial batch coater from CemeCon AG. Two metallic Ce–Gd targets (90:10 at.%) with purity 99.9% and size 88 × 500 mm^2 were sputtered in mixed Ar/O$_2$ atmosphere. The purity of the applied gasses were 99.999%. The coatings were grown on 20 × 20 mm^2 metal-supported half cells mounted on a stage carrying out a two-fold planetary rotation during deposition. The half cells consisted of a metal support and a ScYSZ (ZrO$_2$ co-doped with Sc$_2$O$_3$ and Y$_2$O$_3$) electrolyte. Before starting the deposition the chamber was pumped down to a base pressure below 1 mPa and the substrates were heated to a temperature slightly higher than the deposition temperature of either 300 °C or 400 °C. The total pressure was 0.4 Pa during deposition. A pulsed DC power supply (Advanced Energy, Pinnacle II) delivered 2 kW to each sputtering target with a repetition frequency of 50 kHz and a duty cycle of 50%. Before the deposition series, the voltage hysteresis loop for the system was determined. The films were deposited operating in the transition region between the

metallic and poisoned state of the targets in order to obtain both high deposition rate and stoichiometric films. In order to run the system in the transition region, the cathode current was used as an oxygen partial-pressure feedback signal for controlling the reactive sputtering process. A pulsed DC bias with a frequency of 350 kHz and a reverse time of 1 μs was applied to the mounting stage/samples and used to vary the kinetic energy of ions bombarding the growing film. In order to study the influence of deposition parameters on the ability of the GDC barrier coatings to prevent Sr diffusion, three sets of depositions were performed where the substrate bias voltage, deposition temperature, and film thickness were varied, respectively.

The metal-supported half cells used in this work were fabricated by tape casting of the metal-support (a 22% Cr-based stainless steel alloy), the cermet backbone and the ScYSZ electrolyte followed by co-sintering in a reducing H$_2$/Ar atmosphere under proprietary conditions above 1000 °C. The active fuel cell anode was formed by infiltrating the porous metal-support and cermet with the electrocatalytic active $Ce_{0.8}Gd_{0.2}O_{1.9}$ and Ni. The fabrication procedure and infiltration route of the metal-supported half-cells is described in detail elsewhere [19]. After deposition of the GDC barrier coating on the ScYSZ electrolyte layer, cathodes with a composition of 50 vol.% GDC–50 vol.% LSC $(La_{0.6}Sr_{0.4})_{0.99}CoO_{3−\delta})$ were printed with an area of 0.5 cm^2. The cathode layer was fired in situ in air flow during the cell test start-up at a maximum temperature of 800 °C.

The cells were tested in a set-up also described in Ref. [3]. Platinum meshes placed in parallel with the cell were used to contact the cell to the set-up, and the fuel and oxidant gas was supplied to the cell via alumina tubes perpendicular to the cell active area. Polarization curves were collected at 650 °C, with fuel consisting of 4 vol.% H$_2$O–96 vol.% H$_2$ on the anode side, and air or O$_2$ on the cathode side, and using flows of 100 ml min^{-1} (equivalent to 6 L h^{-1}).

Scanning electron microscopy (SEM, Nova 600 nanoSEM from FEI) was performed on cross-sections of the samples in order to determine the thickness and morphology of the GDC barrier. In order to prepare the samples for SEM they were either vacuum embedded in Epofix (Struers, Denmark), and polished to 1 μm or simply broken into two pieces. Scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDX) were performed on film cross-sections using a Tecnai G2 TF 20 U-Twin 200 kV FEGTEM from FEI. Cross-section samples were prepared by mechanically polishing down to a thickness of approximately 55 μm followed by ion milling using Precision Ion Polishing System (PIPS; Gatan) operated at 5 keV and 5° incident angle with argon ions and a final polishing step at 2 keV for 10 min. X-ray diffraction (XRD) measurements in the θ–2θ geometry were carried out with a Bruker D8 Discover diffractometer using CuKα radiation. Single-line profile analysis was performed with the TOPAS 2.1 [20] software using a pseudo-Voigt peak profile [21]. The size of the coherently diffracting domains, which was used as a measure for the average grain size, and the microstrain were determined from the integral breadths of the Lorentzian and Gaussian constituents of the pseudo-Voigt function, respectively.

A few as-deposited GDC barriers were annealed in a tube furnace (Heraeus, Ro 4/25) in an Ar atmosphere in order to study effect of elevated temperatures on the film microstructure.

3. Results and discussion

3.1. Influence of adatom mobility on the GDC barrier

In order to study the effect of adatom mobility on the ability of the GDC barrier to prevent Sr diffusion, two series of depositions were carried out where either the substrate bias or the deposition

temperature was varied. The application of elevated deposition temperatures or bias voltages are two different ways of providing energy to the growing film. For the study of the effect of bias voltage, films with a thickness of approximately 600 nm were deposited at 400 °C with applied substrate bias voltage of −110 V, −50 V, and at floating potential. Fig. 1 shows SEM images from unpolished cross-sections of the as-deposited films (left) and from polished cross-sections of tested cells containing these films (right). From the unpolished fracture cross-sections it is seen that all films are columnar. When looking at the polished cross-sections the columnar structure is not visible in the GDC barriers deposited at −110 V and −50 V while it is clearly seen in the coating deposited at floating potential. In fact the columnar structure is present in all films (verified by TEM) but cannot be distinguished in polished cross-section of films deposited with applied bias. This reveals that the film deposited at floating potential is less dense than films deposited while applying a bias voltage. The open structure observed at floating potential is due to low adatom mobility during film growth, whereas the films grown under the influence of applied substrate bias becomes denser as energetic gas ions bombard the growing film and increase adatom mobility resulting in better closing of voids [22].

Fig. 2a shows X-ray diffractograms of the films deposited at different bias voltages. Peaks from both the deposited GDC layer and the ScYSZ electrolyte are seen. From the X-ray diffractogram the ScYSZ electrolyte can be seen to consist of randomly oriented grains as all peaks for cubic ScYSZ are seen. All peaks for cubic GDC (ICDD JCP2 No. 75-161) are also present revealing that the GDC is not textured as well. The peak positions from the database are marked by dotted lines. It is seen that all peaks of the as-deposited films are found at slightly lower angles than the reference from the database. This reveals the films are compressively stressed. Table 1 shows average out-of-plane grain sizes and microstrains, as calculated in the single-line profile analysis. The average in grain size is dependent on the grain orientation; however, in general a decreasing grain size is obtained with increasing negative bias voltage. In contrast, the microstrain is seen to increase from ~0.5% at floating potential to above 1% at −50 V and −110 V. This relation
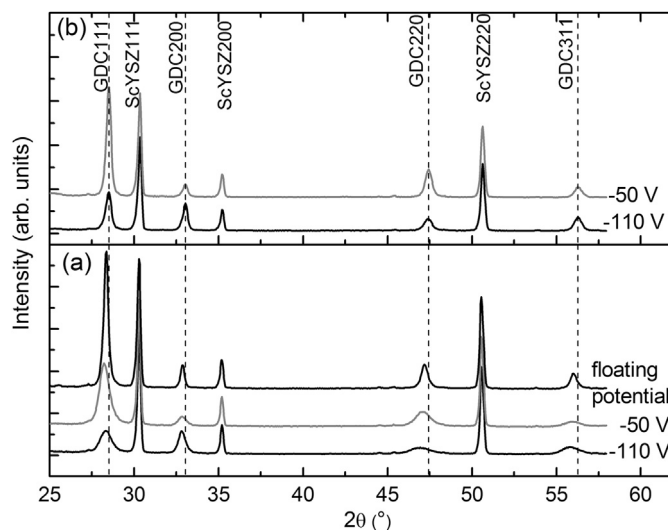

Fig. 2. $\theta-2\theta$ X-ray diffractograms of approximately 0.6 μm GDC deposited at different substrate bias voltage. (a) As-deposited samples, (b) samples annealed at 800 °C for 3 h in an Ar atmosphere. Dotted lines mark positions of GDC peaks in the powder diffractogram (ICDD JCP2 No. 75-161).

is generally seen when preparing films by sputtering using high bias voltages since the energetic ion flux inhibits grain growth and induces defects (microstrain) and compressive stress [22]. It has previously been found that grain size, film stress and microstrain affect the ionic conductivity of GDC and other ionic conductors [23–26]. Investigations have shown the grain size to influence the ionic conduction as grain boundary conductivity was higher than bulk conductivity [27,28] and has therefore been studied as a way of increasing the overall ionic conductivity of SOFC electrolytes [29]. However, the effect of grain size is still debated due to a large scatter in reported results and it has been proposed that other parameters such as lattice strain needs to be considered as well [24]. Studies of stress effects on the ionic conductivity of fluorite
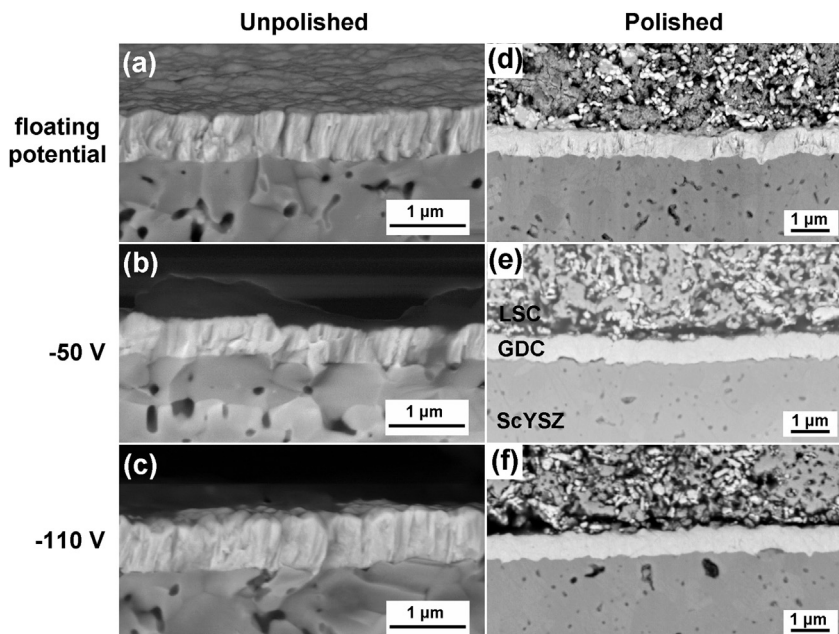

Fig. 1. SEM cross-sections of approximately 0.6 μm thick GDC barriers deposited at floating potential (a, d), −50 V bias (b, e), and −110 V (c, f). (a)–(c) show unpolished cross-sections of untested cells. (c)–(f) show polished cross-sections prepared after cell test.
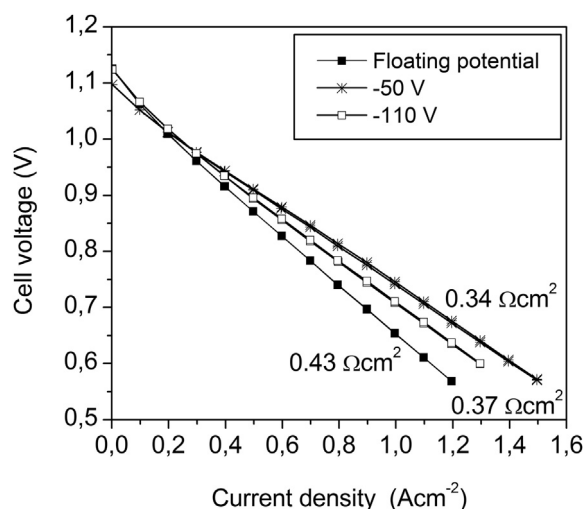
Table 1
Average out-of-plane grain size and microstrain calculated from the X-ray diffractograms for 0.6 μm GDC films deposited at different substrate bias voltage. Calculations have been performed before and after annealing at 800 °C in Ar for 3 h.

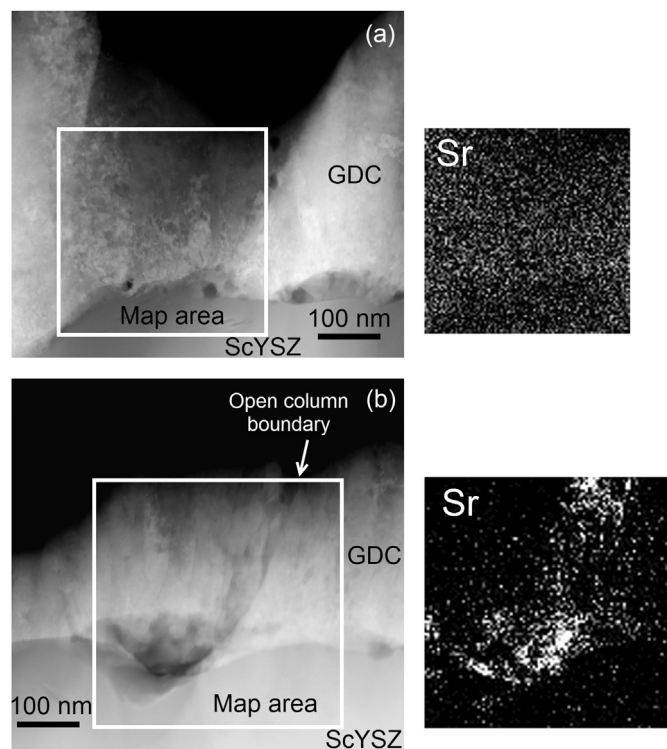| Orientation	Average grain size (nm)	RMS microstrain (%)
Floating potential		
<111>	26.0 ± 1.6	0.4 ± 0.1
<200>	43.8 ± 7.1	0.5 ± 0.1
<220>	19.0 ± 1.2	0.4 ± 0.1
<311>	17.7 ± 1.7	–
−50 V bias		
<111>	13.6 ± 2.2	1.6 ± 0.2
<200>	28.0 ± 14	1.4 ± 0.2
<220>	8.6 ± 1.8	1.2 ± 0.2
<311>	–	–
−110 V bias		
<111>	8.2 ± 3.0	1.3 ± 0.7
<200>	27.7 ± 7.5	1.1 ± 0.1
<220>	–	2.4 ± 0.8
<311>	–	–
−50 V, annealed		
<111>	31.7 ± 4.1	0.6 ± 0.1
<200>	30.4 ± 4.8	0.6 ± 0.1
<220>	28.1 ± 2.6	0.6 ± 0.05
<311>	21.0 ± 3.6	0.5 ± 0.1
−110 V, annealed		
<111>	24.8 ± 4.4	0.8 ± 0.2
<200>	35.4 ± 6.5	0.6 ± 0.1
<220>	19.5 ± 2.6	0.6 ± 0.1
<311>	29.4 ± 6.0	0.6 ± 0.1

structures have shown that a small tensile stress could increase the conductivity [30], while a decrease in conductivity by compressive stress was observed [26]. Elevated temperatures, as the ones the cells are exposed to during cathode sintering and operation, are known to cause stress release and grain growth. Therefore, films deposited at −50 V and −110 V bias were annealed at 800 °C for 3 h. Fig. 2b shows X-ray diffractograms of annealed samples. Compared to as-deposited samples (Fig. 2a) the GDC peak positions have moved to higher angles and are now found at the same angles as the powder reference. This shows the compressive stresses in the films have been released. As seen in Table 1 this treatment also results in grain coarsening and a reduction in microstrain compared to the respective as-deposited samples. After annealing the average grain sizes of the films are comparable which was not the case prior to annealing. The same is seen for the microstrain. As these differences are equalized in the annealing experiment it is reasonable to believe that the same would happen during cathode sintering. Therefore, the deposition-related differences in film stress, grain size, and microstrain are not thought to affect the ionic conductivity in this case.

Polarization curves recorded at 650 °C for button cells with 0.6 μm thick GDC barriers deposited at different substrate bias voltage is shown in Fig. 3. The initial OCV (open circuit voltages) indicated a leak-tight set-up, with an OCV of 1.12 V for floating and −110 V, and 1.10 V for −50 V. For comparison, the theoretical OCV at 650 °C with 4 vol.% H_2O−96 vol.% H_2 as fuel and air as oxidant is 1.11 V, and the observed differences to this value is believed to be due to minor variations in the steam content which is known to affect OCV significantly. The cell containing the GDC barrier deposited at floating potential has the highest area-specific resistance (ASR) of 0.43 Ω cm^2 whereas the ASR values of the cells with GDC barriers deposited at −50 V and −110 V bias are 0.34 Ω cm^2 and 0.37 Ω cm^2, respectively. Comparing the measured ASR to the microstructure of GDC thin films (Fig. 1) it is seen that the film deposited at floating potential has the most open
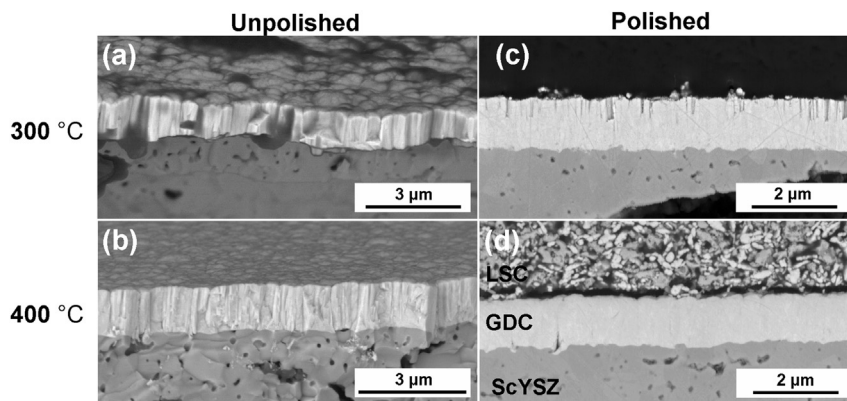

Fig. 3. Electrochemical performance of metal-supported cells with GDC barriers deposited at 400 °C and different substrate bias voltages. The data were recorded at 650 °C with 96% H_2−4% H_2O as fuel and air as oxidant. The inserted numbers are calculated area specific resistances for the cells.

microstructure while films deposited at an applied bias are denser and do not display any significant difference which is replicated in the ASR values. To study the relationship between ASR and microstructure in detail STEM micrographs and EDX mappings of the GDC−ScYSZ interface from samples deposited at floating potential and −50 V substrate bias were obtained, see Fig. 4. Fig. 4a shows STEM/EDX mapping of a cross-section of the film grown at −50 V which displays a dense microstructure. The columnar structure of the film is seen and there are no voids between the columns. Furthermore, the EDX mapping shows that no Sr diffusion

Fig. 4. STEM cross-sections and Sr EDX mappings of approximately 0.6 μm thick GDC barriers deposited at −50 V (a) and floating potential (b).

Fig. 5. SEM cross-sections of approximately 1.2 μm thick GDC barriers deposited at 300 °C (a, c) and 400 °C (b, d). All films are deposited at −50 V substrate bias. (a) and (b) show unpolished cross-sections of untested cells. (c) and (d) show polished cross-sections prepared after cell test.

has taken place. Fig. 4b shows a cross-section of a sample deposited at floating potential which has a more open microstructure. The micrograph has been acquired at a position of an open column boundary that may be comparable to the ones observed in Fig. 1d. The EDX mapping shows Sr diffusion has taken place at this position. Therefore, the high ASR obtained with a barrier deposited at floating potential can be related to the formation of $SrZrO_3$ at the GDC−YSZ interface as the open microstructure fails to stop Sr diffusion along the column boundaries in sputtered GDC films. This is in accordance with the results seen in our previous study of Sr diffusion in a model system imitating an SOFC setup [18].

The difference in ASR between the films deposited at −50 V and −110 V is 0.03 Ω cm^2 which is too small to attribute it to differences in the GDC layer with certainty, and 0.03 Ω cm^2 is within the uncertainty that can be related to other cell components such as small deviations in the anode and cathode performance. For comparison, it should be noted that a cell with a spin-coated GDC barrier under similar condition has an ASR of 0.50 Ω cm^2 meaning the sputtered barriers provide a considerable improvement as previously reported [3].

Approximately 1.2 μm thick films were deposited at −50 V substrate bias and 300 °C and 400 °C in order to study the temperature effect on adatom mobility and the film densification it provides. −50 V bias was chosen, as this bias voltage had shown
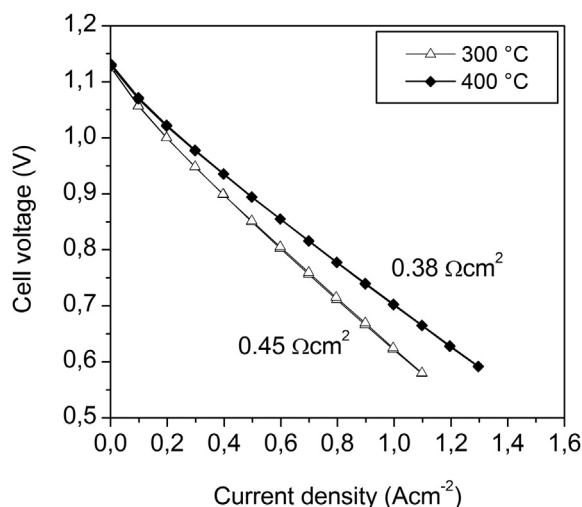
good results in cell tests as seen in Fig. 3. The film thickness was doubled in comparison to the study on the effect of bias voltage to gain information on the influence of film thickness as well. Fig. 5 displays cross-sectional SEM images of deposited GDC coatings. In both cases the unpolished cross-sections (Fig. 5a and b) show the deposited films are columnar but the columns of the film deposited at 300 °C are more easily distinguished. In the polished cross sections (Fig. 5c and d) the columnar structure is still visible in the film deposited at 300 °C whereas it is not observed in the film deposited at 400 °C which shows the film deposited at 300 °C to be less dense.

Polarization curves for cells with GDC barriers deposited at 300 °C and 400 °C, respectively, is seen in Fig. 6. The cell having a GDC barrier deposited at 300 °C is seen to have the highest ASR of 0.45 Ω cm^2 compared to 0.38 Ω cm^2 for the cell with the GDC barrier deposited at 400 °C. The high ASR of the first mentioned cell is comparable to the ASR of the cell with a GDC barrier deposited at 400 °C but without the application of substrate bias (0.43 Ω cm^2, see Fig. 3). A columnar structure of the GDC barriers is also visible in the polished SEM cross-sections for both of these cells (Fig. 1d and 5c). Therefore, it is reasonable to believe the same mechanism of Sr diffusion to the YSZ−GDC interface along column boundaries in the underdense film causes the high ASR.
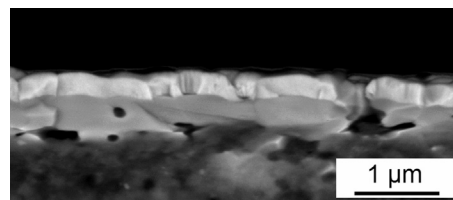
In this study, the use of metal-supported cells sets 400 °C as the upper limit for the deposition temperature as the oxygen present for the reactive deposition process may oxidize the metal-support at elevated temperatures which will reduce cell performance. Therefore, it is irrelevant for the present study if higher temperatures can further densify the barrier.

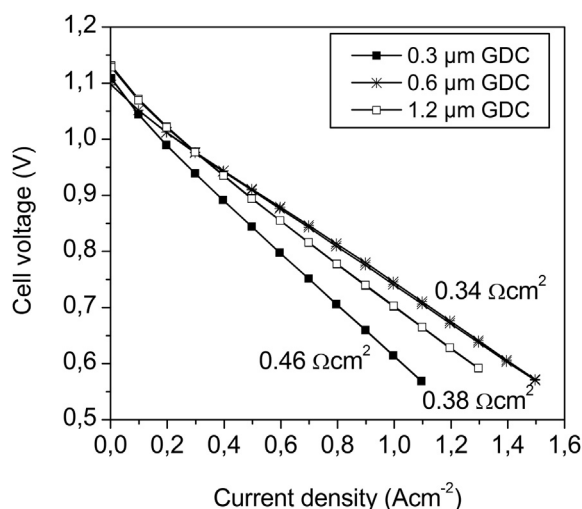### 3.2. Influence of film thickness on the GDC barrier

The influence of GDC film thickness was investigated by depositing films with different thicknesses at −50 V substrate bias and 400 °C. Fig. 7 shows an unpolished SEM cross section of a 0.3 μm thick GDC coating. Comparable films at other thicknesses

Fig. 6. Electrochemical performance of metal-supported cells with approximately 1.2 μm thick GDC barriers deposited at −50 V bias and different temperatures. The data were recorded at 650 °C with 96% H$_2$−4% H$_2$O as fuel and air as oxidant. The inserted numbers are calculated area specific resistances for the cells.

Fig. 7. Unpolished SEM cross-section of an approximately 0.3 μm thick GDC barrier deposited at 400 °C and −50 V substrate bias.

Fig. 8. Electrochemical performance of metal-supported cells with different thickness GDC barriers. The data were recorded at 650 °C with 96% H_2–4% H_2O as fuel and air as oxidant. The inserted numbers are calculated area specific resistances for the cells.

are seen in Fig. 1b (0.6 μm) and Fig. 5b (1.2 μm). A columnar structure is clearly visible at for the 0.6 μm and 1.2 μm thick films while it is less visible for the 0.3 μm thick film. All polished cross-sections (not shown for the 0.3 μm thick film) appear featureless. In contrast to the thicker films, the 0.3 μm film shown in Fig. 7 is not dense as it is too thin to provide an adequate coverage of surface defects in the substrate.

Fig. 8 shows polarization curves for cells containing GDC barriers of different thicknesses. The cell having a 0.3 μm thick GDC barrier has the highest ASR of 0.46 Ω cm^2 while the ASR of the other cells were 0.38 Ω cm^2 (1.2 μm GDC barrier) and 0.34 Ω cm^2 (0.6 μm GDC barrier). The high ASR measured for the cell with 0.3 μm GDC can be related to the incomplete coverage of this barrier which allows Sr diffusion and zirconate formation. The increase in ASR as the thickness is doubled from 0.6 μm to 1.2 μm cannot be ascribed the increased ohmic resistance of the thicker GDC layer. In literature the conductivity of GDC in generally stated to be around 0.03 S cm^{-1} at 650 °C [31,32] which means a thickness increase of 600 nm would result in an ASR increase in the range of 0.002 Ω cm^2 meaning most of the difference of 0.04 Ω cm^2 is related to other cell components. Based on these observations it seems that while 0.3 μm GDC is too thin to effectively avert Sr diffusion, 0.6 μm GDC prevents the diffusion. Any further increase in GDC thickness does not improve performance as the 0.6 μm thick layer has effectively prevented Sr diffusion. This is of interest from a production point of view as unnecessary materials use and process time can be reduced.

4. Conclusion

GDC thin films have been deposited onto ScYSZ electrolytes and implemented into metal-supported SOFCs. In order to optimize the electrochemical performance of the cells the influence of bias voltage, deposition temperature and GDC layer thickness was studied.

Films grown at floating potential were found to have an open microstructure in contrast to films deposited with an applied bias that could activate adatom diffusion and produce denser films. As a result, an area specific resistance (ASR) of 0.43 Ω cm^2 was measured in cell test for a film deposited at floating potential whereas a film deposited at −50 V bias gave an ASR of 0.34 Ω cm^2. STEM/EDX

investigations showed Sr diffusion to occur along the open column boundaries which is in accordance with results of our previous study of Sr diffusion in a model system. Besides densifying the films bias voltage also resulted in smaller grain sizes and induced microstrain and compressive stress in the film. However, heat treatment of the samples resulted in stress release, grain coarsening and reduction of defects (microstrain) which made the microstructure of the films comparable meaning that these as-deposited film differences had no effect after cathode sintering.

Deposition temperature was seen to have a large impact on the adatom mobility and subsequently film density. Films deposited as 300 °C and 400 °C had ASR values of 0.45 Ω cm^2 and 0.38 Ω cm^2, respectively and SEM images showed the microstructure of the film deposited at 300 °C to be less dense. Temperatures above 400 °C were not investigated as it was not desired to go to higher temperatures in order to prevent oxidation damages to the metal-support during the deposition process.

It was found that 0.6 μm of GDC effectively blocked Sr diffusion when depositions were carried out at 400 °C and with the application of bias. 0.3 μm of GDC was not enough to properly cover the substrate due to surface roughness and resulted in a high ASR. For films thicker than 0.6 μm no further improvement of the electrochemical performance was seen as the Sr diffusion was already stopped by the initial 0.6 μm of GDC.

Acknowledgments

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